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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,113	07/12/2000	Pai-Hung Pan	2915.3US (96-0149.2)	1710

7590 04/19/2004

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EXAMINER	
DEO, DUY VU NGUYEN	
ART UNIT	**PAPER NUMBER**
1765	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/614,113	PAN ET AL.
	Examiner	Art Unit
	DuyVu n Deo	1765

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6,7 and 17-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6,7 and 17-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/12/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 6, 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomozawa et al. (US 4,782,037) and Segawa et al. (US 5,428,244).

Tomozawa describes a method for forming a gate stack comprising: forming a gate insulating film 8 on a silicon substrate (col. 3, line 21-25, line 49-54); forming a polysilicon layer 9A having an impurity on top of the gate insulating layer (col. 3, line 60-68); depositing a metallic silicide layer atop the polysilicon layer (claimed metallic silicide film in a non-annealed state) (col. 3, line 63-68); depositing an insulating film (claimed dielectric cap) over the metallic silicide film at a temperature of around 400 degrees Celsius (claimed temperature is sufficient low to maintain the metallic silicide film in the non-anneal state) (col. 4, line 38-40; col. 5, line 45-48). Unlike claimed invention, Tomozawa is silent about the impurity in the polysilicon is formed by ion implantation. However, using ion implantation for this step is well known and practiced by one skill in the art in forming the gate stack as shown here by Segawa (col. 7, line 12-20). Therefore, it would have been obvious for one skill in the art at the time of the invention to form the impurity in the polysilicon in light of Segawa because Segawa describes further step that is silent by Tomozawa in order to form impurity in the polysilicon with a reasonable expectation of success.

Referring to claim 7, this temperature of depositing the insulating film 11 at 400 degree Celsius would be sufficiently low to preclude formation of silicon clusters in metallic silicide film.

3. Claims 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tomozawa and Segawa, and further in view of Chang et al. (US 5,438,006).

Referring to claim 17, Tomozawa further describes patterning the polysilicon, the metallic silicide film (claimed etching the metallic and polysilicon layer) (col. 8, line 65-68) and removing the insulating layer 11 (claimed etching the dielectric cap) (col. 11, line 36-40). Unlike claimed invention, applied prior art of Tomozawa and Segawa do not describe the step of forming and patterning a resist on the dielectric cap and stripping the resist layer. Chang teaches a method for forming gate stack where a resist is formed and patterned on an insulating layer and removed in a conventional manner (claimed stripping the resist) (col. 2, line 35-45). It would have been obvious for one skill in the art at the time of the invention in light of Chang to use a resist layer because as shown in Chang the resist is used as a mask in order to pattern and etch other layers including the insulating layer.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 19-22 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant

art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The specification doesn't describe that a gate stack can be formed consisting essentially the steps cited in claim 19. As shown by the specification, in order to form a gate stack, other essential steps must be done including etching the dielectric, metallic silicide, and polysilicon layer, and activating gate impurities.

6. The applied prior art, taken either alone or in combination, fails to disclose or render obvious a method for forming a gate stack consist essentially of the steps in claim 19. Applied prior art requires other essential steps such as patterning and etching the metallic, polysilicon in order to form a

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DuyVu n Deo whose telephone number is 571-272-1462. The examiner can normally be reached on 6:00-3:30; with alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DVD
4/16/04

DD